In response to the Office Action mailed May 26, 2005, Applicant respectfully requests the consideration of the following remarks and, accordingly, the reconsideration of the Final Rejection of the claims. It is respectfully submitted that the pending claims are in condition for allowance.

REMARKS

Status of the Claims

The claims now pending are claims 1-5, 10-14, 16-17, and 20.

This represents a reduction in the number of claims from eighteen to thirteen, a reduction of five claims, or 22 percent.

Summary of the Invention

Applicants' invention is a circuit for correlating an input signal. The circuit has a parallel array of processing elements. Each of these processing elements comprises a series of analog sampling unit processing elements, where each of the analog sampling unit processing element comprises a sample and hold device for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor.

The circuit also includes a timing circuit for causing the timing signal to be presented in time-delayed succession to successive ones of the analog sampling unit processing elements. The timing circuit has a timing element in parallel with an associated analog sampling unit processing element. The timing element has a phase lock loop or a delay lock loop.

The circuit also includes means for multiplying the output of each analog sample unit processing element. This is to scale the output and sum the scaled outputs of the processing elements.

The Rejections

In the Office Action of May 26, 2005 all of the claims were rejected under as shown in the table, citing U.S. Patent 4,475,170 to Haque et al. and U.S. Patent 5,563,819 to Nelson et al..

Claim No	Haque et al. 102(b)	Nelson et al. 102(b)	Haque et al. 103(a)	Haque et al. + Backgroun d 103(a)	Nelson et al. 103(a)	Nelson et al. + Backgroun d 103(a)
1	X	X				
2			X		X	
3			X		X	
4	X	X				
5			X		X	
10				X		X
11				X		X
12				X		X
13				X		X
14				X		X
16				X		X
17				X		X
20	X	X				

Haque et al. was said to teach a parallel array of processing elements, where each processing element contains an analog sampling circuit, a multiplier, timing switches, and summing means. Haque et al. was also said to teach scaling features corresponding to the coefficients in a Fourier series approximation, and a timing circuit with a plurality of delay elements.

Nelson et al. was said to teach a parallel array of processing elements with an analog sampling circuit, multiplier, timing circuit, and summing means. Nelson et al. was also said to teach scaling features corresponding to the coefficients in a Fourier series approximation, and a timing circuit with a plurality of delay elements.

The References

U.S. Patent 4,475,170 to Haque et al. describes a programmable transversal filter utilizing a plurality of programmable multipliers. The results of each individual multiplication are summed by a summing circuit, to provide an output signal.

Haque et al.'s circuit has a delay network comprising a plurality of signal sample and hold circuits. These are selectively connected to the input bus in sequence. This is so that one sample and hold circuit may store an analog signal sampled during the present time instant, with other sample and hold circuits storing a plurality of analog signals each of which has been sampled during a corresponding one of a plurality of preceding sample periods.

The filter also includes a plurality of reference sample and hold circuits which store error voltages equal to the error voltage component of the voltages provided by the signal sample and hold circuits.

One aspects of Haque et al.'s disclosure is a first analog cross-point switch where each of the plurality of time delayed analog signals may be selectively applied to a selected multiplying means. The filter tap weights remain fixed in the multipliers until reprogrammed, without the need for rotating the tap weights.

A second analog cross-point switch is utilized to selectively connect the output voltage from the reference sample and hold circuits to the multiplier means. This eliminates the effect of the error voltages on the output voltage of the transversal filter.

U.S Patent 5,563,819 to Nelson et al. describes a high precision fast finite impulse response (FIR) filter. The filter periodically samples an analog input signal and holds a

sequentially-replaced number of the resulting discrete-time analog values in fixed storage cells while each value is being multiplied by a number of digital weights.

Nelson et al.'s discrete-time analog values are not passed through delay devices and therefore do not degrade. The weights are stored in a memory or shift register and supplied to the multipliers in a repeating sequence. A predetermined number of the weights are set to zero to increase the setup time of the analog multipliers thereby increasing the precision without slowing the clocking frequency.

Issue

The sole issue presented is whether the pending claims, as amended, are properly allowable to Applicants over Nelson et al. or Haque et al., either alone or taken together, or either of them taken with Applicant's "Background of the Invention."

Argument

Summary of The Argument

Claim 1 is representative of the claims, and has been amended as follows:

> A circuit for correlating an input signal comprising:
> a parallel array of processing elements, each of said processing elements comprising [an] a series of analog sampling ~~circuit~~ unit processing elements, each analog sampling unit processing element comprising a sample and hold device for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor;
> a timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said analog sampling unit processing elements, said timing circuit comprising a timing element in parallel with an associated

analog sampling unit processing element, and said timing element comprising a phase lock loop or a delay lock loop; and,

means for multiplying the output of each analog sample unit processing element to scale the output and summing the scaled ~~output~~ outputs of said processing elements.

Where the following amendments have been made to claim 1:

1) Characterizing each of the processing elements (element 10 of Figure 1) as a series of analog sampling unit processing elements.

2) Each analog sampling unit processing element is characterized as comprising a sample and hold device for sampling the input signal in response to a timing signal.

3) A timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said analog sampling unit processing elements.

4) The timing circuit is claimed as comprising a timing element in parallel with an associated analog sampling unit processing element.

5) The timing element is claimed as comprising a phase lock loop or a delay lock loop.

6) Circuitry for multiplying the output of each analog sample unit processing element to scale the output and summing the scaled outputs of the processing elements.

How Claims Limitations Distinguish Over The Art

Applicants' invention is a circuit for correlating an input signal. The circuit has a parallel array of processing elements. Each of these processing elements comprises a series of analog sampling unit processing elements, where each of the analog sampling unit

processing element comprises a sample and hold device for sampling the input signal in response to a timing signal, and a circuit for scaling the resulting sample according to a predetermined scaling factor.

The circuit also includes a timing circuit for causing the timing signal to be presented in time-delayed succession to successive ones of the analog sampling unit processing elements. The timing circuit has a timing element in parallel with an associated analog sampling unit processing element. The timing element has a phase lock loop or a delay lock loop.

The circuit also includes means for multiplying the output of each analog sample unit processing element. This is to scale the output and sum the scaled outputs of the processing elements.

1) Each of the processing elements (element 10 of Figure 1) is a series of analog sampling unit processing elements.

This element is described at page 8, lines 9-24 as:

> Fig. 1 illustrates the preferred embodiment of the invention based on the processing of analog samples of the input signal. A unit processing element 10 is formed from the combination of a sample and hold device (SHA) 11, an analog multiplier 12 and a constant term C_n that can be represented in a constant fashion as the value of current source, resistor or similar; or as a programmable element in form of a register and digital to analog converter (DAC). The constants C_n represent the coefficients of the Fourier series approximation of the frequency response of the signal to be detected.
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> Each unit processing element 10 is configured to sample the input signal A_{in} and apply the sample to the analog multiplier 12, the other input coming from the constant (or semi-constant DAC/register) element C_n. A plurality of unit processing elements 10 are arrayed to sample the analog input signal successively in time. The output of the multiplier is configured to sum into a common bus 13. The bus may be a simple pair of nodes, the output of the analog multiplier being a differential current into these nodes, or any other means by which an inherent summation can be made to occur.

By way of contrast, Haque et al. describes the sampling element at column 3, line 64 to column 4, line 53, as follows:

FIG. 2 shows a schematic diagram of one embodiment of a four stage transversal filter 10 constructed in accordance with this invention. In practice, the programmable transversal filters constructed in accordance with this invention will have a large number of stages, typically several tens, although the following discussion regarding the four stage filter of FIG. 2 will describe the operation of this invention.

An analog input signal X(t) is applied to input terminal 9 of transversal filter 10. Switches 11, 12, 13 and 14 selectively connect the input signal X(t) to one of the sample and hold circuits S.sub.1 through S.sub.4. The operation of switches 11 via 14 is timed to cause the switches 11 through 14 to operate in sequence, such that at time t.sub.1, X(t.sub.1) is stored through closed switch 11 in sample and hold circuit S.sub.1, at time t.sub.2, analog signal X(t.sub.2) is stored via closed switch 12 in sample and hold circuit S.sub.2, at time t.sub.3 signal X(t.sub.3) is stored via closed switch 13 in sample and hold circuit S.sub.3, and at time t.sub.4 signal X(t.sub.4) is stored via closed switch 14 in sample and hold circuit S.sub.4. In this manner, at any time t, analog signal X(t), X(t-1), X(t-2), and X(t-3) will be stored in sample and hold circuits S.sub.1 through S.sub.4, although the location of signal X(t) and the time delayed signals X(t-1), X(t-2) and X(t-3) within sample and hold circuits S.sub.1 through S.sub.4 will vary with time. This is depicted in Table I.

The operation of the programmable transversal filter 10 of FIG. 2 is as follows, and will be easily understood in conjunction with Table I. First, the tap weights (i.e., multiplying factors) are loaded into multiplying means M.sub.1 through M.sub.4 (having tap weights of a.sub.1 through a.sub.4, respectively) in a well-known manner which will be more fully described later. Then, at time t.sub.1, switch 11 closes and switches 12, 13 and 14 are open, thus storing X(t.sub.1) in sample and hold circuit S.sub.1. At time t.sub.2, switch 12 closes and switches 11, 13 and 14 are open, thus storing X(t.sub.2) in sample and hold circuit S.sub.2. At time t.sub.3, switch 13 closes and switches 11, 12 and 14 are open, thus storing X(t.sub.3) in sample and hold circuit S.sub.3. Similarly at time t.sub.4, switch 14 closes and switches 11, 12 and 13 open, thus storing X(t.sub.4) in sample and hold circuit S.sub.4. At time t.sub.5, switch 11 closes and X(t.sub.5) is stored in sample and hold circuit S.sub.1, with the original signal X(t.sub.1) stored in sample and hold circuit S.sub.1 being lost. Another way of looking at this storage technique is that at time t.sub.5, sample and hold circuit S.sub.1 stores X(t.sub.5), sample and hold circuit S.sub.4 has stored X(t.sub.4), sample and hold circuit S.sub.3 has stored X(t.sub.3), and sample and hold circuit S.sub.2 has stored X(t.sub.2).

The operation of cross-point switch 51 is depicted in FIG. 2. The switches shown in analog cross-point switch 51 are shown as N channel metal oxide silicon (MOS) transistors, although any suitable switch means may be used. Utilizing N channel transistors, a high voltage (logical one) applied to the gate of the transistor causes it to conduct, while a low voltage (logical zero) applied to the gate causes it to turn off. A single logical one is applied to terminals A.sub.0 through A.sub.3 at any one time.

The structure of Haque et al.'s sample and hold circuit and multiplier is materially then Applicants' claim sample and hold elements.

Nelson et al. describes this element at column 5, line 14 to column 7, line 50, as follows:

FIG. 3 is a block diagram of an FIR circuit that is constructed according to the present invention. The analog input signal source 10 is connected in parallel to N sampling devices 40 43. The output of sampling device 40 is connected to the input of hold (storage) device 50. The output of storage device 50 is connected by line 160 to the first multiplying (multiplicand) input of analog multiplier 60. The output (product) of multiplier 60 is connected by line 360 to an input of summing device 90. The output line 400 of summing device 90 carries the discrete time output signal from the filter. In a similar manner, sampling devices 41 43 are connected to storage devices 51 53 and lines 161 163 connect storage devices 51 53 to multipliers 61 63. Multipliers 61 63 are connected to summing device 90 by lines 361 363. The second multiplying (multiplier) inputs of multipliers 60 63 are connected by lines 260 263 to the digital storage unit 70. Controller 80 is connected to sampling devices 40 43 by control lines 240 243 and to the digital storage unit 70 by control line 170.

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FIG. 5 is a schematic diagram of an exemplary embodiment of the present invention. Analog signal source 10 is connected to buffer amplifier 17. The output of the buffer amplifier is connected in parallel to N analog switches 45 48. The output of analog switch 45 is connected by line 165 to storage capacitor 55 and to the first multiplying input of analog multiplier 65. Similarly, switches 46 48 are connected by lines 166 168 to capacitors 56 58 and to multipliers 66 68. The outputs of multipliers 65 68 are connected by lines 365 368 to summing device 90. The output signal line 400 of summing device 90 carries the discrete time output signal of the filter. Line 265 connects multiplier 65 to one cell of an M by N bit shift register 75 where M is the number of bits (width) in the digital word in each cell and N is the number of cells (length) in the register. Shift register 75 has a recirculation path 76 connected from its data output to its data input. Input lines 266 268 of multipliers 66 68 are connected to the remaining cells in shift register 75. Controller 85 is connected to switches 45 48 by control lines 245 248, to shift register 75 by control line 175, and to multipliers 66 68 by line 185.

In operation, the analog input signal from source 10 is input to buffer amplifier 17 which provides isolation for input signal source 10 from the effects of the sampling process and provides sufficient power to charge the storage capacitors 55 58 without distortion of the input waveform. Analog switches 45 48, under timing control from controller 85, periodically connect the output of buffer amplifier 17 to sample storage capacitors 65 68. The sampling frequency is a function of the complexity of the input waveform and is often many times higher than the input frequency. During each sample period, one switch is closed for a time sufficiently long for its capacitor to charge to the instantaneous value of the input voltage but short relative to the rate of change of the input voltage. Each capacitor is thereby charged to the value of the input voltage during the time its switch is closed and retains that value until the next time its switch closes. The switches close one at a time in sequence until all N capacitors have been charged and then the cycle repeats indefinitely.

Nelson et al.'s structure for addressing and charging the storage elements is materially different from Applicants' disclosed

2) Each analog sampling unit processing element is characterized as comprising a sample and hold device for sampling the input signal in response to a timing signal.

This element is also described at page 8, lines 9-16 as:

> Fig. 1 illustrates the preferred embodiment of the invention based on the processing of analog samples of the input signal. A unit processing element 10 is formed from the combination of a sample and hold device (SHA) 11, an analog multiplier 12 and a constant term C_n that can be represented in a constant fashion as the value of current source, resistor or similar; or as a programmable element in form of a register and digital to analog converter (DAC). The constants C_n represent the coefficients of the Fourier series approximation of the frequency response of the signal to be detected.

By way of contrast, Haque et al. describes the sampling element at column 3, line 64 to column 4, line 53, as follows:

> FIG. 2 shows a schematic diagram of one embodiment of a four stage transversal filter 10 constructed in accordance with this invention. In practice, the programmable transversal filters constructed in accordance with this invention will have a large number of stages, typically several tens, although the following discussion regarding the four stage filter of FIG. 2 will describe the operation of this invention.
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> An analog input signal X(t) is applied to input terminal 9 of transversal filter 10. Switches 11, 12, 13 and 14 selectively connect the input signal X(t) to one of the sample and hold circuits S.sub.1 through S.sub.4. The operation of switches 11 via 14 is timed to cause the switches 11 through 14 to operate in sequence, such that at time t.sub.1, X(t.sub.1) is stored through closed switch 11 in sample and hold circuit S.sub.1, at time t.sub.2, analog signal X(t.sub.2) is stored via closed switch 12 in sample and hold circuit S.sub.2, at time t.sub.3 signal X(t.sub.3) is stored via closed switch 13 in sample and hold circuit S.sub.3, and at time t.sub.4 signal X(t.sub.4) is stored via closed switch 14 in sample and hold circuit S.sub.4. In this manner, at any time t, analog signal X(t), X(t-1), X(t-2), and X(t-3) will be stored in sample and hold circuits S.sub.1 through S.sub.4, although the location of signal X(t) and the time delayed signals X(t-1), X(t-2) and X(t-3) within sample and hold circuits S.sub.1 through S.sub.4 will vary with time. This is depicted in Table I.

The actual sample and hold elements and the structure and circuit for storing a signal is disclosed with reference to Figure 6 by Haque et al.. This is a MOSFET circuit (216) and is materially different from Applicants' structure.

Nelson et al. describes this element at column 5, line 14 to column 7, line 50, as follows:

FIG. 3 is a block diagram of an FIR circuit that is constructed according to the present invention. The analog input signal source 10 is connected in parallel to N sampling devices 40 43. The output of sampling device 40 is connected to the input of hold (storage) device 50. The output of storage device 50 is connected by line 160 to the first multiplying (multiplicand) input of analog multiplier 60. The output (product) of multiplier 60 is connected by line 360 to an input of summing device 90. The output line 400 of summing device 90 carries the discrete time output signal from the filter. In a similar manner, sampling devices 41 43 are connected to storage devices 51 53 and lines 161 163 connect storage devices 51 53 to multipliers 61 63. Multipliers 61 63 are connected to summing device 90 by lines 361 363. The second multiplying (multiplier) inputs of multipliers 60 63 are connected by lines 260 263 to the digital storage unit 70. Controller 80 is connected to sampling devices 40 43 by control lines 240 243 and to the digital storage unit 70 by control line 170.

FIG. 5 is a schematic diagram of an exemplary embodiment of the present invention. Analog signal source 10 is connected to buffer amplifier 17. The output of the buffer amplifier is connected in parallel to N analog switches 45 48. The output of analog switch 45 is connected by line 165 to storage capacitor 55 and to the first multiplying input of analog multiplier 65. Similarly, switches 46 48 are connected by lines 166 168 to capacitors 56 58 and to multipliers 66 68. The outputs of multipliers 65 68 are connected by lines 365 368 to summing device 90. The output signal line 400 of summing device 90 carries the discrete time output signal of the filter. Line 265 connects multiplier 65 to one cell of an M by N bit shift register 75 where M is the number of bits (width) in the digital word in each cell and N is the number of cells (length) in the register. Shift register 75 has a recirculation path 76 connected from its data output to its data input. Input lines 266 268 of multipliers 66 68 are connected to the remaining cells in shift register 75. Controller 85 is connected to switches 45 48 by control lines 245 248, to shift register 75 by control line 175, and to multipliers 66 68 by line 185.

Nelson et al.'s disclosed store and hold is addressed differently then Applicants'.

3) A timing circuit for causing said timing signal to be presented in time-delayed succession to successive ones of said analog sampling unit processing elements.

The timing circuit is described at page 8, line 25, to page 9, line 20

A delay circuit 14 is designed to apply the sample signal D_{in} to the SHA and then apply a known delay in time before passing the signal to the next unit processing element. In this way the SHA devices are made to sample successively in time. Although conveniently done as a cascade of connected elements 15 implemented adjacent to the unit processing elements, the successive sampling means may be provided in any form available to the designer of the system. This application of successive samples may occur very quickly – in the state of the art today the successive sampler may be derived from a chain of gates or similar and the delay between samples therefore made less then 100pS without much difficulty. Those skilled in the art will recognize the need to provide for an interval of time when the sampling device is re-acquiring the signal: this disclosure recognizes that the SHA may require a pair of devices and the description of the SHA element may

therefore consist of the equivalent of two conventional SHA devices. Due to the number M of unit processing elements present, each equivalent sampler is only required to cycle at the signal sampling rate divided by M.

The sampling of the analog sampler array is conveniently provided by use of a time delay (or phase shifting) element 15 adjacent to each analog sampler. The control of the time delaying element, for example using a Delay Lock Loop (or Phase Lock Loop), is well known in the art. Many samples of the input are taken within one operational cycle: each of the unit processing elements samples once in the cycle. The output of the array is equivalent to a single ADC operating at M times the operational cycle rate (where M is the number of sampler elements) in the more conventional ADC and DSP implementation.

Haque et al. describes circuitry for generally achieving this function at column4, lines 4 to 43:

An analog input signal X(t) is applied to input terminal 9 of transversal filter 10. Switches 11, 12, 13 and 14 selectively connect the input signal X(t) to one of the sample and hold circuits S.sub.1 through S.sub.4. The operation of switches 11 via 14 is timed to cause the switches 11 through 14 to operate in sequence, such that at time t.sub.1, X(t.sub.1) is stored through closed switch 11 in sample and hold circuit S.sub.1, at time t.sub.2, analog signal X(t.sub.2) is stored via closed switch 12 in sample and hold circuit S.sub.2, at time t.sub.3 signal X(t.sub.3) is stored via closed switch 13 in sample and hold circuit S.sub.3, and at time t.sub.4 signal X(t.sub.4) is stored via closed switch 14 in sample and hold circuit S.sub.4. In this manner, at any time t, analog signal X(t), X(t-1), X(t-2), and X(t-3) will be stored in sample and hold circuits S.sub.1 through S.sub.4, although the location of signal X(t) and the time delayed signals X(t-1), X(t-2) and X(t-3) within sample and hold circuits S.sub.1 through S.sub.4 will vary with time. This is depicted in Table I.

The operation of the programmable transversal filter 10 of FIG. 2 is as follows, and will be easily understood in conjunction with Table I. First, the tap weights (i.e., multiplying factors) are loaded into multiplying means M.sub.1 through M.sub.4 (having tap weights of a.sub.1 through a.sub.4, respectively) in a well-known manner which will be more fully described later. Then, at time t.sub.1, switch 11 closes and switches 12, 13 and 14 are open, thus storing X(t.sub.1) in sample and hold circuit S.sub.1. At time t.sub.2, switch 12 closes and switches 11, 13 and 14 are open, thus storing X(t.sub.2) in sample and hold circuit S.sub.2. At time t.sub.3, switch 13 closes and switches 11, 12 and 14 are open, thus storing X(t.sub.3) in sample and hold circuit S.sub.3. Similarly at time t.sub.4, switch 14 closes and switches 11, 12 and 13 open, thus storing X(t.sub.4) in sample and hold circuit S.sub.4. At time t.sub.5, switch 11 closes and X(t.sub.5) is stored in sample and hold circuit S.sub.1, with the original signal X(t.sub.1) stored in sample and hold circuit S.sub.1 being lost. Another way of looking at this storage technique is that at time t.sub.5, sample and hold circuit S.sub.1 stores X(t.sub.5), sample and hold circuit S.sub.4 has stored X(t.sub.4), sample and hold circuit S.sub.3 has stored X(t.sub.3), and sample and hold circuit S.sub.2 has stored X(t.sub.2).

The operation of cross-point switch 51 is depicted in FIG. 2. The switches shown in analog cross-point switch 51 are shown as N channel metal oxide silicon (MOS) transistors, although any suitable switch means may be used. Utilizing N channel transistors, a high voltage (logical one) applied to the gate of the transistor causes it to conduct, while a low voltage (logical zero) applied to the gate causes it to turn off. A single logical one is applied to terminals A.sub.0 through A.sub.3 at any one time.

Nelson et al. describes this element at column 5, line 14 to column 7, line 50, as follows:

> FIG. 3 is a block diagram of an FIR circuit that is constructed according to the present invention. The analog input signal source 10 is connected in parallel to N sampling devices 40 43. The output of sampling device 40 is connected to the input of hold (storage) device 50. The output of storage device 50 is connected by line 160 to the first multiplying (multiplicand) input of analog multiplier 60. The output (product) of multiplier 60 is connected by line 360 to an input of summing device 90. The output line 400 of summing device 90 carries the discrete time output signal from the filter. In a similar manner, sampling devices 41 43 are connected to storage devices 51 53 and lines 161 163 connect storage devices 51 53 to multipliers 61 63. Multipliers 61 63 are connected to summing device 90 by lines 361 363. The second multiplying (multiplier) inputs of multipliers 60 63 are connected by lines 260 263 to the digital storage unit 70. Controller 80 is connected to sampling devices 40 43 by control lines 240 243 and to the digital storage unit 70 by control line 170.
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> In operation, controller 80, which provides the sequencing function for the entire filter, repeatedly cycles through N logical states. Each state selects a different sampling device 40 43 and provides timing to the selected device for acquiring a sample and storing it in its associated storage device 50 53. Referring to FIG. 4A, the analog input signal 100S is periodically sampled at the times indicated by the dots on waveform 100S. Each dot represents one sample taken by one of the N sampling devices. Since a different sampling device is selected by each state, each sampling device is active in only one out of each N sample periods. For simplicity, in the following description, FIGS. 4A and 4B are used to show the case where N=4; both FIGS. 4A and 4B show the input signal 100S and output signal 400S for reference while FIG. 4A shows signals resulting from sampling devices 40 and 41 and FIG. 4B shows signals resulting from sampling devices 42 and 43. Sample values resulting from the action of sampling device 40 are stored in storage device 50 and are shown as signal 160S in FIG. 4A; signal 160S appears on line 160 in FIG. 3. Because each sampling device is active only once in N samples, the value of signal 160S stored in storage device 50 only changes once per four samples as shown in FIG. 4A. In a similar manner, the values of signals 161S 163S from sampling devices 41 43, stored in storage devices 51 53, also change once every four sample periods. Because each signal 160S 163S results from the selection of a different sampling device by controller 80, as it repeatedly cycles through N states, each signal changes at a different sample time.
>
> Each state of the controller also selects, via control line 170, a different digital word in digital storage unit 70 to be supplied via line 260 to the second multiplier input of multiplier circuit 60. The signal on line 260, shown as signal 260S in FIG. 4, is the sequence of four weight values. The weight values change during each sample period (signal 260S) while the stored sample values change each four sample periods (signal 160S). In FIGS. 4A and 4B, the numbers below the signal baselines are either the index numbers of the weights (k) or of the sample values (n).
>
> By performing a multiplication of signal 160S by signal 260S during each sample period, all four weights are used to multiply each sample value once each during every cycle of four states. Likewise, each of the other multiplier input lines 261 263 is connected to a different digital word selected by the state of controller 80. In general, with each change of state, controller 80 increments access for each multiplier input line 260 263 to the next higher indexed digital weight; and, when the highest index (k=N 1) weight is accessed by a multiplier input, the next access is to the lowest (k=0) index weight. Multipliers 60 63 then multiply the sample values currently stored in storage devices 50 53 by the weighting

values currently supplied by digital storage unit 70. The resulting product signals on lines 360 363 are then added by summing device 90 and supplied as the output signal 400S.

In short, each discrete time output value y(n) is the product of a vector A, whose elements are the analog values stored in the sample storage devices 50 53, and a vector B, whose analog elements are equal to the digital values stored in the digital storage unit 70. In steady state operation, after the forming of each such product, the oldest element of A is replaced with a new sample and the elements of B are rotated one position.

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FIG. 5 is a schematic diagram of an exemplary embodiment of the present invention. Analog signal source 10 is connected to buffer amplifier 17. The output of the buffer amplifier is connected in parallel to N analog switches 45 48. The output of analog switch 45 is connected by line 165 to storage capacitor 55 and to the first multiplying input of analog multiplier 65. Similarly, switches 46 48 are connected by lines 166 168 to capacitors 56 58 and to multipliers 66 68. The outputs of multipliers 65 68 are connected by lines 365 368 to summing device 90. The output signal line 400 of summing device 90 carries the discrete time output signal of the filter. Line 265 connects multiplier 65 to one cell of an M by N bit shift register 75 where M is the number of bits (width) in the digital word in each cell and N is the number of cells (length) in the register. Shift register 75 has a recirculation path 76 connected from its data output to its data input. Input lines 266 268 of multipliers 66 68 are connected to the remaining cells in shift register 75. Controller 85 is connected to switches 45 48 by control lines 245 248, to shift register 75 by control line 175, and to multipliers 66 68 by line 185.

In operation, the analog input signal from source 10 is input to buffer amplifier 17 which provides isolation for input signal source 10 from the effects of the sampling process and provides sufficient power to charge the storage capacitors 55 58 without distortion of the input waveform. Analog switches 45 48, under timing control from controller 85, periodically connect the output of buffer amplifier 17 to sample storage capacitors 65 68. The sampling frequency is a function of the complexity of the input waveform and is often many times higher than the input frequency. During each sample period, one switch is closed for a time sufficiently long for its capacitor to charge to the instantaneous value of the input voltage but short relative to the rate of change of the input voltage. Each capacitor is thereby charged to the value of the input voltage during the time its switch is closed and retains that value until the next time its switch closes. The switches close one at a time in sequence until all N capacitors have been charged and then the cycle repeats indefinitely.

Each time the input signal from source 10 is sampled, the digital weights in the shift register 75, under timing control from controller 85, advance one position; and, as the word in the last cell of the register is shifted out, it is shifted into the first cell via the recirculation path 76. In this way, with each sample of the input signal, the digital words (weights) rotate one cell position. The digital words are supplied to the digital multiplying inputs of multipliers 65 68 and loaded into the multipliers by the clock signal on line 185. The analog multiplying inputs of multipliers 65 68 are supplied with sample values from storage capacitors 55 58. During each sample period, multipliers 65 68 multiply all N sampled values currently stored in capacitors 55 58 by the weights currently presented by their respective cells in shift register 75. The resulting discrete time analog outputs (products) from multipliers 65 68 are added by summing device 90 and provided as the filter output signal y(n) on line 400.

Haque et al.'s and Nelson et al.'s sampling timing circuit are both different in structure and operation from Applicant's claimed and described phase locked loop/delay locked loop timing circuit

4) The timing circuit is claimed as comprising a timing element in parallel with an associated analog sampling unit processing element.

The timing circuit is also described at page 8, line 25, to page 9, line 20

> A delay circuit 14 is designed to apply the sample signal D_{in} to the SHA and then apply a known delay in time before passing the signal to the next unit processing element. In this way the SHA devices are made to sample successively in time. Although conveniently done as a cascade of connected elements 15 implemented adjacent to the unit processing elements, the successive sampling means may be provided in any form available to the designer of the system. This application of successive samples may occur very quickly – in the state of the art today the successive sampler may be derived from a chain of gates or similar and the delay between samples therefore made less then 100pS without much difficulty. Those skilled in the art will recognize the need to provide for an interval of time when the sampling device is re-acquiring the signal: this disclosure recognizes that the SHA may require a pair of devices and the description of the SHA element may therefore consist of the equivalent of two conventional SHA devices. Due to the number M of unit processing elements present, each equivalent sampler is only required to cycle at the signal sampling rate divided by M.
>
> The sampling of the analog sampler array is conveniently provided by use of a time delay (or phase shifting) element 15 adjacent to each analog sampler. The control of the time delaying element, for example using a Delay Lock Loop (or Phase Lock Loop), is well known in the art. Many samples of the input are taken within one operational cycle: each of the unit processing elements samples once in the cycle. The output of the array is equivalent to a single ADC operating at M times the operational cycle rate (where M is the number of sampler elements) in the more conventional ADC and DSP implementation.

Nelson et al. describes this element at column 5, line 14 to column 7, line 50, as follows:

> In operation, controller 80, which provides the sequencing function for the entire filter, repeatedly cycles through N logical states. Each state selects a different sampling device 40 43 and provides timing to the selected device for acquiring a sample and storing it in its associated storage device 50 53. Referring to FIG. 4A, the analog input signal 100S is periodically sampled at the times indicated by the dots on waveform 100S. Each dot represents one sample taken by one of the N sampling devices. Since a different sampling device is selected by each state, each sampling device is active in only one out of each N sample periods. For simplicity, in the following description, FIGS. 4A and 4B are used to show the case where N=4; both FIGS. 4A and 4B show the input signal 100S and output signal 400S for reference while FIG. 4A shows signals resulting from sampling devices

40 and 41 and FIG. 4B shows signals resulting from sampling devices 42 and 43. Sample values resulting from the action of sampling device 40 are stored in storage device 50 and are shown as signal 160S in FIG. 4A; signal 160S appears on line 160 in FIG. 3. Because each sampling device is active only once in N samples, the value of signal 160S stored in storage device 50 only changes once per four samples as shown in FIG. 4A. In a similar manner, the values of signals 161S 163S from sampling devices 41 43, stored in storage devices 51 53, also change once every four sample periods. Because each signal 160S 163S results from the selection of a different sampling device by controller 80, as it repeatedly cycles through N states, each signal changes at a different sample time.

Each state of the controller also selects, via control line 170, a different digital word in digital storage unit 70 to be supplied via line 260 to the second multiplier input of multiplier circuit 60. The signal on line 260, shown as signal 260S in FIG. 4, is the sequence of four weight values. The weight values change during each sample period (signal 260S) while the stored sample values change each four sample periods (signal 160S). In FIGS. 4A and 4B, the numbers below the signal baselines are either the index numbers of the weights (k) or of the sample values (n).

By performing a multiplication of signal 160S by signal 260S during each sample period, all four weights are used to multiply each sample value once each during every cycle of four states. Likewise, each of the other multiplier input lines 261 263 is connected to a different digital word selected by the state of controller 80. In general, with each change of state, controller 80 increments access for each multiplier input line 260 263 to the next higher indexed digital weight; and, when the highest index (k=N 1) weight is accessed by a multiplier input, the next access is to the lowest (k=0) index weight. Multipliers 60 63 then multiply the sample values currently stored in storage devices 50 53 by the weighting values currently supplied by digital storage unit 70. The resulting product signals on lines 360 363 are then added by summing device 90 and supplied as the output signal 400S.

In short, each discrete time output value y(n) is the product of a vector A, whose elements are the analog values stored in the sample storage devices 50 53, and a vector B, whose analog elements are equal to the digital values stored in the digital storage unit 70. In steady state operation, after the forming of each such product, the oldest element of A is replaced with a new sample and the elements of B are rotated one position.

5) The timing element is claimed as comprising a phase lock loop or a delay lock loop.

The timing circuit is also described at page 9, lines 13-20:

The sampling of the analog sampler array is conveniently provided by use of a time delay (or phase shifting) element 15 adjacent to each analog sampler. The control of the time delaying element, for example using a Delay Lock Loop (or Phase Lock Loop), is well known in the art. Many samples of the input are taken within one operational cycle: each of the unit processing elements samples once in the cycle. The output of the array is equivalent to a single ADC operating at M times the operational cycle rate (where M is the number of sampler elements) in the more conventional ADC and DSP implementation.

Neither Nelson et al. nor Haque et al. describes the use of a delay lock loop or a delay lock loop to effect timing.

6) Circuitry for multiplying the output of each analog sample unit processing element to scale the output and summing the scaled outputs of the processing elements.

The multiplication circuitry is described at page 8, lines 9-16:

> Fig. 1 illustrates the preferred embodiment of the invention based on the processing of analog samples of the input signal. A unit processing element 10 is formed from the combination of a sample and hold device (SHA) 11, an analog multiplier 12 and a constant term C_n that can be represented in a constant fashion as the value of current source, resistor or similar; or as a programmable element in form of a register and digital to analog converter (DAC). The constants C_n represent the coefficients of the Fourier series approximation of the frequency response of the signal to be detected.

Haque et al. et al's multiplication circuitry is described at column 4, line 61 – to column 5, line 18:

> As shown in Table I, at time t.sub.1 with a logical one applied to terminal A.sub.0, and logical zeroes applies to terminals A.sub.1 through A.sub.3, sample and hold circuit S.sub.1 is connected to multiplier M.sub.1, sample and hold circuit S.sub.2 is connected to multiplier M.sub.4, sample and hold circuit S.sub.3 is connected to multiplier M.sub.3, and sample hold circuit S.sub.4 is connected to multiplier M.sub.2.
>
> At time t.sub.2, a logical one is applied to terminal A.sub.1, with terminals A.sub.0, A.sub.2 and A.sub.3 being held low (logical zero). Thus, sample and hold circuit S.sub.2 is connected to multiplier M.sub.1, sample and hold circuit S.sub.3 is connected to multiplier M.sub.4, sample and hold circuit S.sub.4 is connected to multiplier M.sub.3, and sample and hold circuit S.sub.1 is connected to multiplier M.sub.2. the address signals applied to terminals A.sub.0 through A.sub.3, and the resultant connections between sample and hold circuits S.sub.1 through S.sub.4 to multipliers M.sub.1 through M.sub.4, are shown in Table I for times t.sub.1 through t.sub.4.
>
> Thus, as shown in Table I, the output voltage from multiplier M.sub.1 during each time t.sub.1 through t.sub.4 is equal to a.sub.1 X(t); the output voltage from multiplier M.sub.2 is equal to a.sub.2 X(t-1); the output voltage from multiplier M.sub.3 is equal to a.sub.3 X(t-2); and the output voltage from multiplier M.sub.4 is equal to a.sub.4 X(t-3). Thus, as shown in Table I, at all times t.sub.1 through t.sub.4 the output voltage y(t) from summing means 7 available on terminal 8 is equal to
>
> y(t)=a.sub.1 X(t)+a.sub.2 X(t-1)+a.sub.3 X(t-2)+a.sub.4 X(t-3) (3)

which is the output voltage desired from a transversal filter.

Nelson et al. describes this element at column 5, line 14 to column 7, line 50, as follows:

> FIG. 3 is a block diagram of an FIR circuit that is constructed according to the present invention. The analog input signal source 10 is connected in parallel to N sampling devices 40 43. The output of sampling device 40 is connected to the input of hold (storage) device 50. The output of storage device 50 is connected by line 160 to the first multiplying (multiplicand) input of analog multiplier 60. The output (product) of multiplier 60 is connected by line 360 to an input of summing device 90. The output line 400 of summing device 90 carries the discrete time output signal from the filter. In a similar manner, sampling devices 41 43 are connected to storage devices 51 53 and lines 161 163 connect storage devices 51 53 to multipliers 61 63. Multipliers 61 63 are connected to summing device 90 by lines 361 363. The second multiplying (multiplier) inputs of multipliers 60 63 are connected by lines 260 263 to the digital storage unit 70. Controller 80 is connected to sampling devices 40 43 by control lines 240 243 and to the digital storage unit 70 by control line 170.
>
> In operation, controller 80, which provides the sequencing function for the entire filter, repeatedly cycles through N logical states. Each state selects a different sampling device 40 43 and provides timing to the selected device for acquiring a sample and storing it in its associated storage device 50 53. Referring to FIG. 4A, the analog input signal 100S is periodically sampled at the times indicated by the dots on waveform 100S. Each dot represents one sample taken by one of the N sampling devices. Since a different sampling device is selected by each state, each sampling device is active in only one out of each N sample periods. For simplicity, in the following description, FIGS. 4A and 4B are used to show the case where N=4; both FIGS. 4A and 4B show the input signal 100S and output signal 400S for reference while FIG. 4A shows signals resulting from sampling devices 40 and 41 and FIG. 4B shows signals resulting from sampling devices 42 and 43. Sample values resulting from the action of sampling device 40 are stored in storage device 50 and are shown as signal 160S in FIG. 4A; signal 160S appears on line 160 in FIG. 3. Because each sampling device is active only once in N samples, the value of signal 160S stored in storage device 50 only changes once per four samples as shown in FIG. 4A. In a similar manner, the values of signals 161S 163S from sampling devices 41 43, stored in storage devices 51 53, also change once every four sample periods. Because each signal 160S 163S results from the selection of a different sampling device by controller 80, as it repeatedly cycles through N states, each signal changes at a different sample time.
>
> Each state of the controller also selects, via control line 170, a different digital word in digital storage unit 70 to be supplied via line 260 to the second multiplier input of multiplier circuit 60. The signal on line 260, shown as signal 260S in FIG. 4, is the sequence of four weight values. The weight values change during each sample period (signal 260S) while the stored sample values change each four sample periods (signal 160S). In FIGS. 4A and 4B, the numbers below the signal baselines are either the index numbers of the weights (k) or of the sample values (n).
>
> By performing a multiplication of signal 160S by signal 260S during each sample period, all four weights are used to multiply each sample value once each during every cycle of four states. Likewise, each of the other multiplier input lines 261 263 is connected to a different digital word selected by the state of controller 80. In general, with each change of state, controller 80 increments access for each multiplier input line 260 263 to the next higher indexed digital weight; and, when the highest index (k=N 1) weight is accessed by

a multiplier input, the next access is to the lowest (k=0) index weight. Multipliers 60 63 then multiply the sample values currently stored in storage devices 50 53 by the weighting values currently supplied by digital storage unit 70. The resulting product signals on lines 360 363 are then added by summing device 90 and supplied as the output signal 400S.

In short, each discrete time output value y(n) is the product of a vector A, whose elements are the analog values stored in the sample storage devices 50 53, and a vector B, whose analog elements are equal to the digital values stored in the digital storage unit 70. In steady state operation, after the forming of each such product, the oldest element of A is replaced with a new sample and the elements of B are rotated one position.

The filter described for FIG. 3 implements the following mathematical function. This function is the same as that presented in the description for FIG. 1 except that the terms are rearranged as indicated below in the example equations. ##EQU3##

For example, if N=4,

$y(n)=W(0)x(n)+W(1)x(n\ 1)+W(2)x(n\ 2)+W(3)x(n\ 3).$

Then, if $x(n\ k)=0$ for $n\ k<0$, after rearranging the terms,

$y(0)=W(0)x(0)$

$y(1)=W(1)x(0)+W(0)x(1)$

$y(2)=W(2)x(0)+W(1)x(1)+W(0)x(2)$

$y(3)=W(3)x(0)+W(2)x(1)+W(1)x(2)+W(0)x(3)$

$y(4)=W(0)x(4)+W(3)x(1)+W(2)x(2)+W(1)x(3)$

$y(5)=W(1)x(4)+W(0)x(5)+W(3)x(2)+W(2)x(3)$

$y(6)=W(2)x(4)+W(1)x(5)+W(0)x(6)+W(3)x(3)$

$y(7)=W(3)x(4)+W(2)x(5)+W(1)x(6)+W(0)x(7)$

and the sequence continues indefinitely.

FIG. 5 is a schematic diagram of an exemplary embodiment of the present invention. Analog signal source 10 is connected to buffer amplifier 17. The output of the buffer amplifier is connected in parallel to N analog switches 45 48. The output of analog switch 45 is connected by line 165 to storage capacitor 55 and to the first multiplying input of analog multiplier 65. Similarly, switches 46 48 are connected by lines 166 168 to capacitors 56 58 and to multipliers 66 68. The outputs of multipliers 65 68 are connected by lines 365 368 to summing device 90. The output signal line 400 of summing device 90 carries the discrete time output signal of the filter. Line 265 connects multiplier 65 to one cell of an M by N bit shift register 75 where M is the number of bits (width) in the digital word in each cell and N is the number of cells (length) in the register. Shift register 75 has a recirculation path 76 connected from its data output to its data input. Input lines 266 268 of multipliers 66 68 are connected to the remaining cells in shift register 75. Controller 85 is connected to switches 45 48 by control lines 245 248, to shift register 75 by control line 175, and to multipliers 66 68 by line 185.

In operation, the analog input signal from source 10 is input to buffer amplifier 17 which provides isolation for input signal source 10 from the effects of the sampling process and provides sufficient power to charge the storage capacitors 55 58 without distortion of the input waveform. Analog switches 45 48, under timing control from controller 85, periodically connect the output of buffer amplifier 17 to sample storage capacitors 65 68. The sampling frequency is a function of the complexity of the input waveform and is often many times higher than the input frequency. During each sample period, one switch is closed for a time sufficiently long for its capacitor to charge to the instantaneous value of the input voltage but short relative to the rate of change of the input voltage. Each capacitor is thereby charged to the value of the input voltage during the time its switch is closed and retains that value until the next time its switch closes. The switches close one at a time in sequence until all N capacitors have been charged and then the cycle repeats indefinitely.

Each time the input signal from source 10 is sampled, the digital weights in the shift register 75, under timing control from controller 85, advance one position; and, as the word in the last cell of the register is shifted out, it is shifted into the first cell via the recirculation path 76. In this way, with each sample of the input signal, the digital words (weights) rotate one cell position. The digital words are supplied to the digital multiplying inputs of multipliers 65 68 and loaded into the multipliers by the clock signal on line 185. The analog multiplying inputs of multipliers 65 68 are supplied with sample values from storage capacitors 55 58. During each sample period, multipliers 65 68 multiply all N sampled values currently stored in capacitors 55 58 by the weights currently presented by their respective cells in shift register 75. The resulting discrete time analog outputs (products) from multipliers 65 68 are added by summing device 90 and provided as the filter output signal y(n) on line 400.

Summary

The scope of the invention is defined by the metes and bounds of the explicit language of the claims. Neither Haque et al. nor Nelson et al., either alone, or in combination with each other, or in combination with the "Background of the Invention" teach or suggest the claimed invention. The combination of these six elements in amended claim 1 is neither taught nor suggested by the art of record. Thus, the claims are properly allowable to the Applicants.

More then just the mere presence or absence of all of the elements, or any sub set of them, the references fail to teach the effect of the combination.

CONCLUSION

Claims 1-5, 10-14, 16-17, and 20 are pending. Applicants respectfully submit that, in view of the discussion set forth herein, the pending claims are patentable over the prior art.

The Commissioner is hereby instructed to charge any additional fees due or credit any overpayment to Deposit Account No. 50-2421.

If there are any questions regarding this correspondence, please contact the undersigned at (408) 288-7588.

Respectfully submitted,

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